WHAT IS CLAIMED IS:

1. A decoding apparatus configured to decode compression-encoded video data in units of at least one block, the video data including a variable length code comprising:

a variable length decoder which decodes the variable length code to output a zero-run length and a nonzero coefficient;

an inverse quantizer which inverse-quantizes the nonzero coefficient to output an inverse-quantized result;

a zero-run reconstruction processor which reconstruct zero coefficients, the zero coefficients corresponding to the zero-run length;

a FIFO (First-In First-Out) memory arranged between the inverse quantizer and the zero-run reconstruction processor and configured to store the zero-run length data and nonzero coefficients, the memory operating with first-in first-out and having a memory capacity for storing coefficients contained in a plurality of blocks;

an inverse discrete cosine transformer which subjects the reconstructed coefficients and inverse-quantized coefficient to an inverse discrete cosine transformation to output a transformed result; and

a motion compensator which subjects the transformed result to a motion compensation.

2. An apparatus according to claim 1, wherein the variable length decoder decodes the variable length code corresponding to a macro block including the given number of blocks.

3. An apparatus according to claim 1, wherein the zero-run reconstruction device includes a buffer memory configured to write in the zero coefficients and nonzero coefficients therein at a write-in speed and read out them therefrom at a readout speed higher than the write-in speed.

4. An apparatus according to claim 1, wherein if nonzero coefficient does not exist at a final position of a block when the inverse quantizer receives a block end signal indicating the end of the block from the variable length decoder, the inverse quantizer generates a zero coefficient as the final DCT coefficient of the block.

5. An apparatus according to claim 1, wherein the variable length decoder stops its output in units of one block when the inverse quantizer is unreceivable the zero-run length and nonzero coefficient from the variable length decoder.

6. An apparatus according to claim 1, wherein every time the inverse quantizer receives the zero-run length from the variable length decoder, the inverse quantizer accumulates a value obtained by adding "1" to the zero-run length and generates scan address data

indicating a coefficient position of the nonzero coefficient, to generate quantization step size data every coefficient position based on the scan address data and scan pattern data indicating the scan pattern.

7. An apparatus according to claim 6, wherein the inverse quantizer outputs to the first-in first-out memory DCT coefficient data indicating the inverse quantization result, the scan address data indicating a position of the DCT coefficient and the scan pattern data.

8. An apparatus according to claim 7, wherein the inverse quantizer stops its output in units of one coefficient when the FIFO memory is unreceivable the data from the inverse quantizer.

9. An apparatus according to claim 1, wherein the zero-run reconstruction processor includes an internal scan address counter increased one by one for each clock, and rejects next data input from the FIFO memory until a scan address received from the FIFO memory has coincided with a count value of the internal scan address counter, to generate the zero coefficients corresponding to the zero-run length.

10. An apparatus according to claim 3, wherein when the buffer memory writes in 58 to 62 percents of all coefficients corresponding to one block, the buffer memory reads out the coefficients.

11. An apparatus according to claim 1, which

includes an intra-DC reconstruction device configured to reproduce DC components contained in the coefficients in intra-blocks in parallel with inverse quantization of the inverse quantizer.

12. A decoding apparatus configured to decode compression-encoded video data including a variable length code, comprising:

a plurality of decompression devices configured to decompress compression-encoded video data corresponding to a plurality of channels, respectively, each of the decompression devices including:

a variable length decoder which decodes the variable length code to output a zero-run length and a nonzero coefficient;

an inverse quantizer which inverse-quantizes the nonzero coefficient to output an inverse-quantized result;

a zero-run reconstruction processor which reconstruct zero coefficients corresponding to the zero-run length; and

a FIFO (First-In First-Out) memory arranged between the inverse quantizer and the zero-run reconstruction processor and configured to store the zero-run length data and nonzero coefficients, the memory operating with first-in first-out and having a memory capacity for storing coefficients contained in a plurality of blocks;

a plurality of parameter extractors provided corresponding to the decoding processors, and configured to generate parameters concerning one macro-block every time the variable length decoder included in each of the decoding processors completes decoding of one block; and

an inverse discrete cosine transformer which subjects the coefficients from the decoding processors to inverse discrete cosine transformation to obtain transformed coefficients; and

a motion compensator which subjects the transformed coefficients to a motion compensation in accordance with the parameters concerning one block input from the parameter extractors alternately.

13. An apparatus according to claim 12, wherein the variable length decoder decodes the variable length code corresponding to a macro block including a predetermined number of blocks.

14. An apparatus according to claim 12, wherein the zero-run reconstruction device includes a buffer memory configured to write in the zero coefficients and nonzero coefficients therein at a write-in speed and read out them therefrom at a readout speed higher than the write-in speed.

15. An apparatus according to claim 12, wherein if nonzero coefficient does not exist at a final position of a block when the inverse quantizer receives a block

end signal indicating the end of the block from the variable length decoder, the inverse quantizer generates a zero coefficient as the final DCT coefficient of the block.

16. An apparatus according to claim 12, wherein the variable length decoder stops its output in units of one coefficient when the inverse quantizer is unreceivable the zero-run length and nonzero coefficient from the variable length decoder.

17. An apparatus according to claim 12, wherein every time the inverse quantizer receives the zero-run length from the variable length decoder, the inverse quantizer accumulates a value obtained by adding "1" to the zero-run length and generates scan address data indicating a coefficient position of the nonzero coefficient, to generate quantization step size data every coefficient position based on the scan address data and scan pattern data indicating the scan pattern.

18. An apparatus according to claim 12, wherein the zero-run reconstruction processor includes an internal scan address counter increased one by one for each clock, and rejects next data input from the FIFO memory until a scan address received from the FIFO memory has coincided with a count value of the internal scan address counter, to generate the zero coefficients corresponding to the zero-run length.

19. An apparatus according to claim 12, which

includes an intra-DC reconstruction device configured to reproduce DC components contained in the coefficients in intra-blocks in parallel with inverse quantization of the inverse quantizer.